

---

**Features of 80186, 80286,  
80386, 80486**

**and**

**Pentium family processors**

**EE VI Sem**

**Amit Thakur**

---

---

# 80186 Basic Features

- The 80186 contains 16 – bit data bus
  - The internal register structure of 80186 is virtually identical to the 8086
  - About the only difference is that the 80186 contain additional reserved interrupt vectors and some very powerful built-in I/O features
-

---

## **Clock Generator:**

- The internal clock generator replaces the external 8284A clock generator used with the 8086 microprocessors. This reduces the component count in a system

## **Programmable Interrupt Controller:**

- The PIC arbitrates all internal and external interrupts and controls up to two external 8259A PICs. When an external 8259 is attached, the 80186 microprocessors function as the master and the 8259 functions as the slave
-

---

## **Timers:**

- The timer section contains three fully programmable 16-bit timers
  - The timers 0 and 1 generate wave-forms for external use and driven by either the master clock of the 80186 or by an external clock
  - The third timer, timer 2 is internal and clocked by the master clock
-

---

## **Programmable DMA Unit:**

- The programmable DMA unit contains two DMA channels, or four DMA channels in some models
  - Each channel can transfer data between memory locations, between memory and IO, or between IO devices
-

---

## **Programmable chip selection unit:**

- The chip selection is a built-in programmable memory and I/O decoder
  - It has 6 output lines to select memory, 7 lines to select I/O
-

---

## **Power save/Power Down Feature:**

- The power save feature allows the system clock to be divided by 4, 8, or 16 to reduce power consumption
  - The power saving feature is started by software and exited by a hardware event such as an interrupt
-

---

## **Refresh Control Unit:**

- The refresh control unit generates the refresh row address at the interval programmed
-



---

# 80286 Basic Features

- The 80286 microprocessor is an advanced version of the 8086 microprocessor that is designed for multi user and multitasking environments
  - The 80286 addresses 16 M Byte of physical memory and 1G Bytes of virtual memory by using its memory-management system
  - The 80286 is basically an 8086 that is optimized to execute instructions in fewer clocking periods than the 8086
-

- 
- Like the 80186, the 80286 doesn't incorporate internal peripherals; instead it contains a memory-management unit (MMU)
  - The 80286 operates in both the real and protected modes
  - In the real mode, the 80286 addresses a 1MByte memory address space and is virtually identical to 8086
  - In the protected mode, the 80286 addresses a 16MByte memory space
-

- 
- The clock is provided by the 82284 clock generator, and the system control signals are provided by the 82288 system bus controller
  - The 80286 contains the same instructions except for a handful of additional instructions that control the memory-management unit
-

---

# 80386 Basic Features

- The 80386 microprocessor is an enhanced version of the 80286 microprocessor and includes a memory-management unit is enhanced to provide memory paging
  - The 80386 also includes 32-bit extended registers and a 32-bit address and data bus
  - The 80386 has a physical memory size of 4GBytes that can be addressed as a virtual memory with up to 64TBytes
-

- 
- The 80386 is operated in the pipelined mode, it sends the address of the next instruction or memory data to the memory system prior to completing the execution of the current instruction
  - This allows the memory system to begin fetching the next instruction or data before the current is completed
  - This increases access time, thus reducing the speed of the memory
-

- The I/O structure of the 80386 is almost identical to the 80286, except that I/O can be inhibited when the 80386 is operated in the protected mode through the I/O bit protection map
  - The register set of the 80386 contains extended versions of the registers introduced on the 80286 microprocessor. These extended registers include EAX, EBX, ECX, EDX, EBP, ESP, EDI, ESI, EIP and EFLAGS
  - The instruction set of the 80386 is enhanced to include instructions that address the 32-bit extended register set
-

- Interrupts, in the 80386 microprocessor, have been expanded to include additional predefined interrupts in the interrupt vector table
  - The 80386 memory manager is similar to the 80286, except the physical addresses generated by the MMU are 32 bits wide instead of 24-bits
  - The 80386 is also capable of paging
  - The 80386 is operated in the real mode (i.e. 8086 mode) when it is reset
-

- 
- The real mode allows the microprocessor to address data in the first 1MByte of memory
  - In the protected mode, 80386 addresses any location in its 4G bytes of physical address space
-



# 80486 Basic Features

- The 80486 microprocessor is an improved version of the 80386 microprocessor that contains an 8K-byte cache and an 80387 arithmetic co processor; it executes many instructions in one clocking period
- The 80486 microprocessor executes a few new instructions that control the internal cache memory

- 
- A new feature found in the 80486 in the BIST (built-in self-test) that tests the microprocessor, coprocessor, and cache at reset time
  - If the 80486 passes the test, EAX contains a zero
  - Additional test registers are added to the 80486 to allow the cache memory to be tested
  - These new test registers are TR3 (cache data), TR4 (cache status), and TR5 (cache control)
-

---

# Pentium Processor basic features

- The Pentium microprocessor is almost identical to the earlier 80386 and 80486 microprocessors
  - The main difference is that the Pentium has been modified internally to contain a dual cache (instruction and data) and a dual integer unit
  - The Pentium also operates at a higher clock speed of 66 MHz
-

- 
- The data bus on the Pentium is 64 – bits wide and contains eight byte-wide memory banks selected with bank enable signals
  - Memory access time, without wait states, is only about 18 ns in the 66 MHz Pentium
  - The superscalar structure of the Pentium contains three independent processing units: a floating point processor and two integer processing units
-

- 
- A new mode of operation called the System Memory Management (SMM) mode has been added to the Pentium. It is intended for high-level system functions such as power management and security
  - The Built-in Self-test (BIST) allows the Pentium to be tested when power is first applied to the system
  - Allows 4MByte memory pages instead of the 4KByte pages
-

---

# Pentium Pro Processor basic features

- The Pentium Pro is an enhanced version of the Pentium microprocessor that contains not only the level 1 caches found inside the Pentium, but the level 2 cache of 256 K or 512K found on most main boards
  - The Pentium Pro operates using the same 66 MHz bus speed as the Pentium and the 80486
  - It uses an internal clock generator to multiply the bus speed by various factors to obtain higher internal execution speeds
-

- 
- The only significant software difference between the Pentium Pro and earlier microprocessors is the addition of FCMOV and CMOV instructions
  - The only hardware difference between the Pentium Pro and earlier microprocessors is the addition of 2M paging and four extra address lines that allow access to a memory address space of 64G Bytes
-